Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A device comprising:

~~a graphics processor that includes:~~

a graphics rendering engine; and

a frame buffer memory, operatively coupled to the graphics rendering engine, that is accessible to a user bus, wherein the frame buffer memory has a defined secure area and an unsecure area; ~~and wherein the graphics processor is configurable as a secure or unsecure processor~~

a plurality of writing clients including a set of authorized writing clients having an ability to write to the secure area and the unsecure area; and

a set of unauthorized writing clients having an ability to write to the unsecure area and lacking an ability to write to the secure area.

2. (original) The device of Claim 1, wherein access to the secure area is controlled by at least one access register defining at least one bound of the secure area.

3. (original) The device of Claim 2, wherein the at least one access register may only be written if the at least one access register is uninitialized.

4. (original) The device of Claim 1, further comprising at least one frame buffer reading client having an ability to read the secure area and at least one unauthorized reading client having an ability to read the unsecure area and lacking an ability to read the secure area.

5. (original) The device of Claim 2, wherein the at least one access register is a one-time programmable register.

6. (canceled)

7. (canceled)

8. (original) The device of Claim 4, further comprising a memory controller that receives a memory access request from a client of the plurality of reading clients and determines an access privilege of the client based on content of a client access privilege register, and selects one of at least refusing access and permitting access.

9. (previously presented) The device of Claim 4, further comprising if the memory controller selects refusing access, the memory controller further selects at least one of denying access, providing of erroneous data, and providing scrambled data.

10. (canceled)

11. (currently amended) The device of Claim [[10]]1, further comprising:

a memory controller that receives an access request from a client of the plurality of clients and

determines an access privilege of the client, and selects at least one of refusing access and permitting access.

12. (currently amended) The device of Claim [[10]]1, wherein:

each client of the set of authorized writing clients has an access privilege allowing the client to write to the secure area and the unsecure area, and

each client of the set of unauthorized writing clients has an access privilege allowing the client to write to the unsecure area and prohibiting the client to write to the unsecure area.

13. (original) The device of Claim 12, wherein the access privileges are determined by a hardware enabling device.

14. (original) The device of Claim 12, wherein the access privileges are hardwired.

15. (original) The device of Claim 12, wherein the access privileges are fusible.

16. (currently amended) A graphics processing apparatus comprising:

a frame buffer memory that is accessible to a user bus;

an encryption/decryption module operatively coupled to the frame buffer memory, the encryption module operative to encrypt data passed to the frame buffer memory and decrypting data passing from the frame buffer memory;

the data is of a data type having a protection level;

the encryption/decryption module is operative to detect the protection level of the data type; and

the encryption/decryption module selectively scrambles data passed to the frame buffer memory and ~~unscrambling~~ unscrambles data passing from the frame buffer memory according to the protection level of the data type.

17. (canceled)

18. (canceled)

19. (previously presented) The apparatus of Claim 16 including a plurality of memory access clients, each client having an access privilege, wherein the encryption/decryption module selectively scrambles data passed to the frame buffer memory and unscrambles data passing from the frame buffer memory according to the access privilege of the client.

20. (currently amended) An integrated circuit for an electronic system, the integrated circuit comprising:

~~a graphics processor that includes:~~

a graphics rendering engine;

a local frame buffer memory coupled to the graphics rendering engine and having a secure area and an unsecure area, the secure area and the unsecure area being accessible by the graphics rendering engine; [[and]]

a user bus interface coupled to the graphics rendering engine and to the local frame buffer memory, the user bus interface operative to couple the integrated circuit to a user bus and to provide access of the unsecure area to the user bus;~~ and wherein the graphics processor is configurable as a secure or unsecure processor~~

a plurality of reading clients including a set of authorized reading clients having an ability to read the secure area and the unsecure area, and a set of unauthorized reading clients having an ability to read the unsecure area and lacking an ability to read the secure area;

a memory access protection module that receives an access request from a client of the plurality of clients and determines an access privilege of the client, and selects one of a set consisting of refusing access and permitting access;

if the memory access protection module selects refusing access, the memory access protection module further selects one of a set consisting of denying access, providing of erroneous data, and providing scrambled data;

wherein the memory access protection module receives an access request from a client of the plurality of clients and determines an access privilege of the client, and selects at least one of refusing access and permitting access; and

wherein each client of the set of authorized writing clients has an access privilege allowing the client to write to the secure area and the unsecure area, and each client of the set of unauthorized writing clients has an access privilege allowing the client to write to the unsecure area and prohibiting the client to write to the unsecure area.

21. (original) The integrated circuit of Claim 20, wherein access to the secure area is controlled by at least one access register defining at least one bound of the secure area.

22. (original) The integrated circuit of Claim 21, wherein the at least one access register may only be written if the at least one access register is uninitialized.

23. (canceled)

24. (original) The integrated circuit of Claim 21, wherein the at least one access register is a one-time programmable.

25. (original) The integrated circuit of Claim 24, wherein the at least one access register is a one-time programmable nonvolatile register.

26. (canceled)

27. (canceled)

28. (canceled)

29. (canceled)

30. (original) The integrated circuit of Claim 29, wherein the access privileges are determined by a hardware enabling device.

31. (original) The integrated circuit of Claim 30, wherein the access privileges are hardwired.

32. (original) The integrated circuit of Claim 30, wherein the access privileges are fusible.

33. (previously presented) The device of claim 1 including a memory controller operatively coupled to the frame buffer memory and operative to pass substituted data back to a requesting client where a memory request by the client is for data in a secure region.

34. (previously presented) A graphics processing apparatus comprising:

a frame buffer memory that is accessible to a user bus;

an encryption/decryption module operatively coupled to the frame buffer memory, the encryption module operative to encrypt data passed to the frame buffer memory and decrypting data passing from the frame buffer memory; and

wherein the data has an address within the frame buffer memory, wherein the encryption/decryption module selectively scrambles data passed to the frame buffer memory and

unscrambles data passing from the frame buffer memory according to whether the address is within a secure range of addresses.

35. (new) The device of claim 1 wherein the ability to write to the secure area and the unsecure area by a writing client and wherein the ability to write to the unsecure area and lacking an ability to write to the secure area by an unauthorized writing client is determined in response to a memory request made by either the writing client or unauthorized writing client.